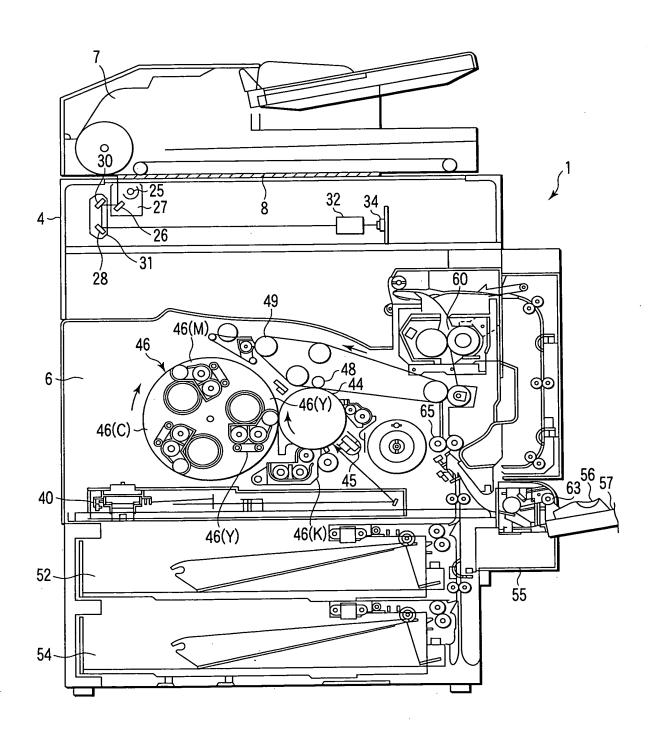


107 External I/F -101 **CPU EtherMAC USB2.0** 103 ,102 **IEEE1284** PCI bus Main System controller memory 115 104 108 Compression accelerator Fax-I/F IDE-I/F System Second expansion circuit 116 bus Second compression circuit 109 Second encoding circuit HDD FAX board Second decoding circuit 106 _105 Image memory controller 110 First decoding First encoding Image memory circuit circuit Operation First expansion First compression panel circuit circuit 114 113 111 112 Image processing Image processing Printer unit Scanner unit circuit circuit

FIG.1



F1G.2

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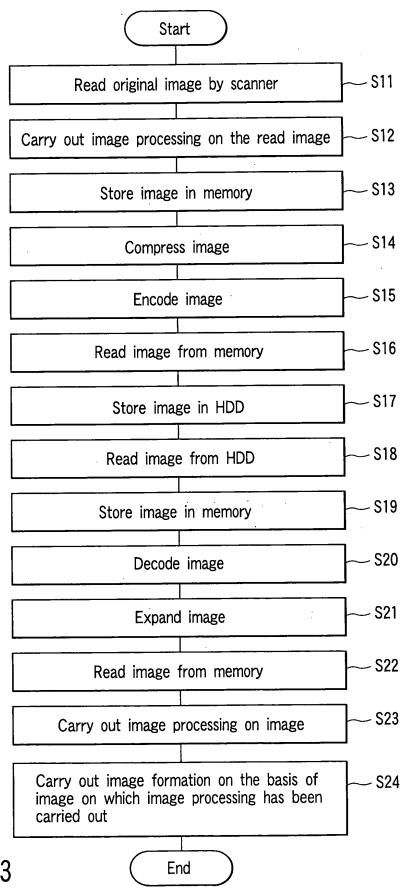


FIG. 3

Start — S31 Receive PDL information via external interface - S32 Store PDL information in main memory **—** S33 Develop PDL information into image information - S34 Store image information in main memory - S35 Compress image Encode image - S36 Read image from memory - S37 - S38 Store image in HDD Read image from HDD - \$39 Store image in memory **- S40** Decode image - S41 Expand image - S42 - S43 Read image from memory - S44 Carry out image processing on image Carry out image formation on the basis of image - S45 on which image processing has been carried out F I G. 4 End

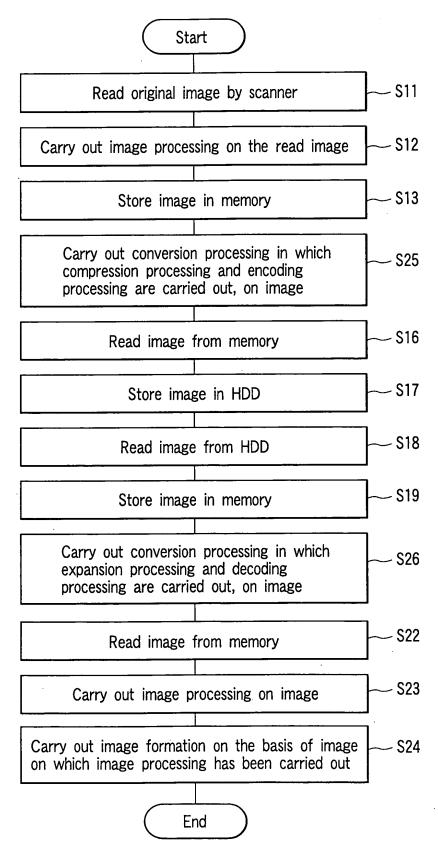


FIG. 5

Appl. No.: 10/804,113

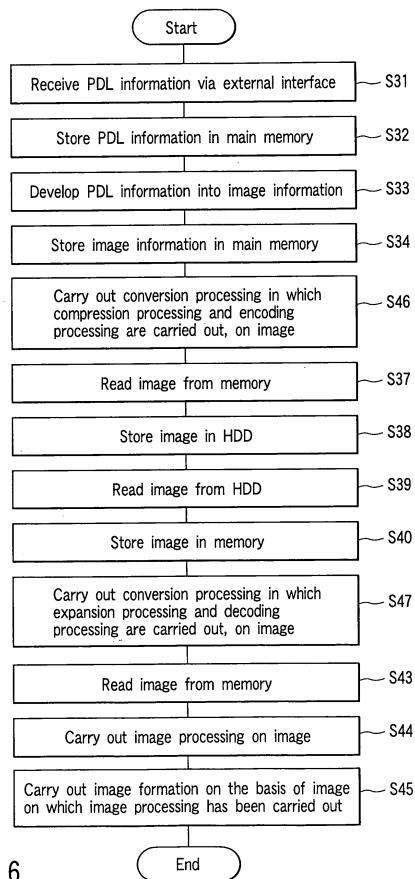


FIG.6